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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,897	10/21/2003	Mitsuhiro Watanabe	OkI.592	3759

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EXAMINER	
GELAGAY, SHEWAYE	
ART UNIT	PAPER NUMBER
2137	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/688,897	WATANABE, MITSUHIRO	
	Examiner	Art Unit	
	Shewaye Gelagay	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 4 recites, "jump to a second address in a first address in said memory". It is unclear how the jump instruction to jump to the second address is given in the first address. Appropriate action is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Art (hereinafter Admission) in view of Katsuta U.S. Patent Number 5,671,394.

As per claims 1 and 3:

Addmission teaches a microcomputer comprising:

a first memory where a normal-operation program is stored; (figure 2, item 2)

a second memory where a functional test program stored; (figure 2, item 3)

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated; (figure 2, item 9)

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated; (figure 2, item 1)

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; (figure 2, item 7; page 3, line 25-page 4, line 3) and

a test circuit which gives a preset specific instruction to said CPU when, in said test mode, a specific memory area has been accessed. (figure 2, item 8; page 4, line 4-page 5, line 13)

Admission does not explicitly disclose a security test signal has been output from said CPU. Katsuta in analogous art, however, discloses a security test signal has been

output from said CPU. (col. 3, line 26-col. 4, line 55) Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the method disclosed by Admission with Katsuta in order to provide ROM data protection which gives a high degree of protection with a minimum amount of hardware. (col. 2, lines 30-31; Katsuta)

As per claim 2:

The combination of Admission and Katsuta teaches all the subject matter as discussed above. In addition, Admission further discloses a microcomputer wherein said specific instruction given to said CPU from said test circuit is a instruction which is to be detected by said memory management unit as an illegitimate access. (page 4, line 4-page 5, line 13)

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Art (hereinafter Admission) in view of Mendell U.S. Patent Number 4,519,032.

As per claim 4:

Admission teaches a test method for a microcomputer having a memory for storing a program, a central processing unit (CPU) which runs said program stored in said memory and a memory management unit which monitors an access to said memory and outputs an interrupt signal to said CPU upon detection of an illegitimate access, said test method sequentially executing:

a process of writing a jump instruction to jump to a second address in a first address in said memory; (page 2, lines 20-23)

a process of setting access to said second address as an illegitimate access in said memory management unit; (page 2, lines 23-27)

a process of determining if there is a failure depending on whether or not said memory management unit has output said interrupt signal as a result of executing said jump instruction written at said first address. (page 2, lines 23-27)

Admission does not explicitly disclose a process of jumping to a first address. Mandell in analogous art, however, discloses a process of jumping to a first address. (col. 4, lines 42-58) Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the method disclosed by Admission with Mendell in order to cause the processor to respond to particular preprogrammed routines upon detection of an interrupt signal. (col. 4, lines 42-45; Mandell)

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shewaye Gelagay whose telephone number is 571-272-4219. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 571-272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shewaye Gelagay SG

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER